

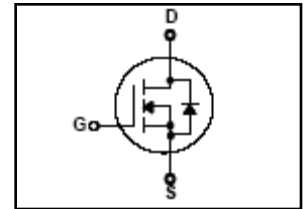
## HF5N65S / HF15N65S 650V N-Channel MOSFET

$BV_{DSS} = 650\text{ V}$   
 $R_{DS(on) \text{ typ}} = 2.3\ \Omega$   
 $I_D = 4.2\text{ A}$

**D<sup>2</sup>-PAK I<sup>2</sup>-PAK**



**HF5N65S HF15N65S**  
1. Gate 2. Drain 3. Source



### FEATURES

- Originative New Design
- Superior Avalanche Rugged Technology
- Robust Gate Oxide Technology
- Very Low Intrinsic Capacitances
- Excellent Switching Characteristics
- Unrivalled Gate Charge : 10.5 nC (Typ.)
- Extended Safe Operating Area
- Lower  $R_{DS(ON)}$  : 2.3  $\Omega$  (Typ.) @  $V_{GS}=10\text{V}$
- 100% Avalanche Tested

### Absolute Maximum Ratings $T_C=25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Value	Units
$V_{DSS}$	Drain-Source Voltage	650	V
$I_D$	Drain Current – Continuous ( $T_C = 25^\circ\text{C}$ )	4.2	A
	Drain Current – Continuous ( $T_C = 100^\circ\text{C}$ )	2.4	A
$I_{DM}$	Drain Current – Pulsed (Note 1)	16.8	A
$V_{GS}$	Gate-Source Voltage	$\pm 30$	V
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)	180	mJ
$I_{AR}$	Avalanche Current (Note 1)	4.2	A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)	10	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.5	V/ns
$P_D$	Power Dissipation ( $T_A = 25^\circ\text{C}$ ) *	3.13	W
	Power Dissipation ( $T_C = 25^\circ\text{C}$ ) - Derate above $25^\circ\text{C}$	100	W
		0.8	W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
$T_L$	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	$^\circ\text{C}$

### Thermal Resistance Characteristics

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	--	1.25	$^\circ\text{C/W}$
$R_{\theta JA}$	Junction-to-Ambient*	--	40	
$R_{\theta JA}$	Junction-to-Ambient	--	62.5	

\* When mounted on the minimum pad size recommended (PCB Mount)

**Electrical Characteristics**  $T_C=25\text{ }^\circ\text{C}$  unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
<b>On Characteristics</b>						
$V_{GS}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	2.5	--	4.5	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\ \text{V}, I_D = 2.1\ \text{A}$	--	2.3	2.9	$\Omega$
<b>Off Characteristics</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\ \text{V}, I_D = 250\ \mu\text{A}$	650	--	--	V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$	--	0.6	--	$\text{V}/^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 650\ \text{V}, V_{GS} = 0\ \text{V}$	--	--	1	$\mu\text{A}$
		$V_{DS} = 520\ \text{V}, T_C = 125^\circ\text{C}$	--	--	10	$\mu\text{A}$
$I_{GSSF}$	Gate-Body Leakage Current, Forward	$V_{GS} = 30\ \text{V}, V_{DS} = 0\ \text{V}$	--	--	100	nA
$I_{GSSR}$	Gate-Body Leakage Current, Reverse	$V_{GS} = -30\ \text{V}, V_{DS} = 0\ \text{V}$	--	--	-100	nA
<b>Dynamic Characteristics</b>						
$C_{iss}$	Input Capacitance	$V_{DS} = 25\ \text{V}, V_{GS} = 0\ \text{V},$ $f = 1.0\ \text{MHz}$	--	520	680	pF
$C_{oss}$	Output Capacitance		--	60	80	pF
$C_{rss}$	Reverse Transfer Capacitance		--	8.0	10.5	pF
<b>Switching Characteristics</b>						
$t_{d(on)}$	Turn-On Time	$V_{DS} = 325\ \text{V}, I_D = 4.2\ \text{A},$ $R_G = 25\ \Omega$  (Note 4,5)	--	11	33	ns
$t_r$	Turn-On Rise Time		--	45	90	ns
$t_{d(off)}$	Turn-Off Delay Time		--	40	88	ns
$t_f$	Turn-Off Fall Time		--	48	100	ns
$Q_g$	Total Gate Charge	$V_{DS} = 520\ \text{V}, I_D = 4.2\ \text{A},$ $V_{GS} = 10\ \text{V}$  (Note 4,5)	--	10.5	13.5	nC
$Q_{gs}$	Gate-Source Charge		--	2.5	--	nC
$Q_{gd}$	Gate-Drain Charge		--	4.0	--	nC
<b>Source-Drain Diode Maximum Ratings and Characteristics</b>						
$I_S$	Continuous Source-Drain Diode Forward Current		--	--	4.2	A
$I_{SM}$	Pulsed Source-Drain Diode Forward Current		--	--	16.8	
$V_{SD}$	Source-Drain Diode Forward Voltage	$I_S = 4.2\ \text{A}, V_{GS} = 0\ \text{V}$	--	--	1.4	V
$t_{rr}$	Reverse Recovery Time	$I_S = 4.2\ \text{A}, V_{GS} = 0\ \text{V}$ $di_F/dt = 100\ \text{A}/\mu\text{s}$ (Note 4)	--	300	--	ns
$Q_{rr}$	Reverse Recovery Charge		--	2.2	--	$\mu\text{C}$

**Notes ;**

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2.  $L=18.9\text{mH}, I_{AS}=4.2\text{A}, V_{DD}=50\text{V}, R_G=25\Omega$ , Starting  $T_J=25^\circ\text{C}$
3.  $I_{SD}\leq 4.2\text{A}, di/dt\leq 200\text{A}/\mu\text{s}, V_{DD}\leq BV_{DSS}$ , Starting  $T_J=25^\circ\text{C}$
4. Pulse Test : Pulse Width  $\leq 300\mu\text{s}$ , Duty Cycle  $\leq 2\%$
5. Essentially Independent of Operating Temperature

Typical Characteristics

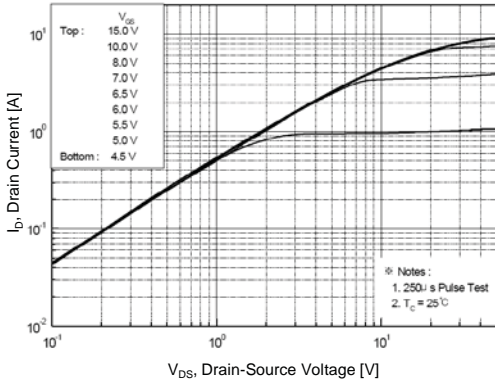


Figure 1. On Region Characteristics

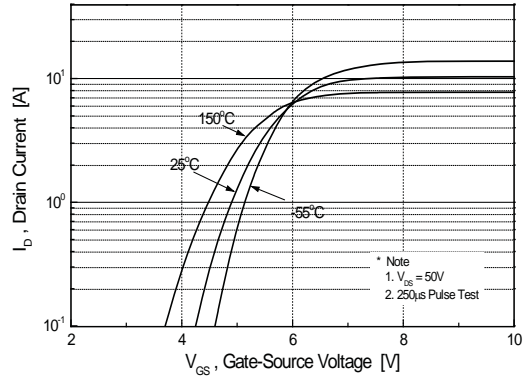


Figure 2. Transfer Characteristics

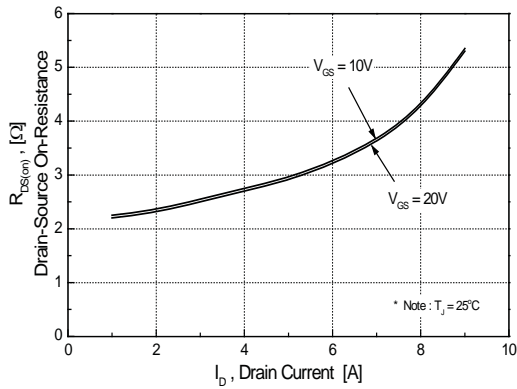


Figure 3. On Resistance Variation vs Drain Current and Gate Voltage

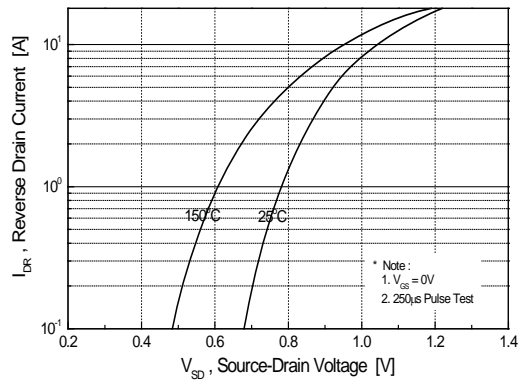


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

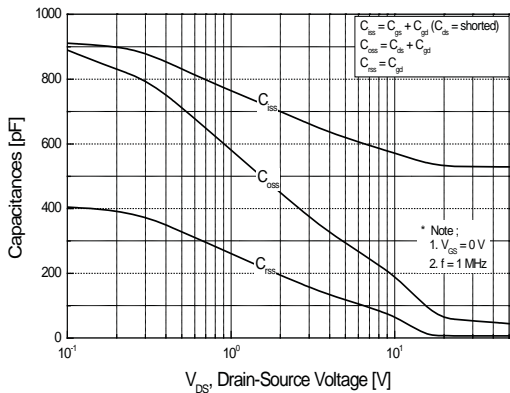


Figure 5. Capacitance Characteristics

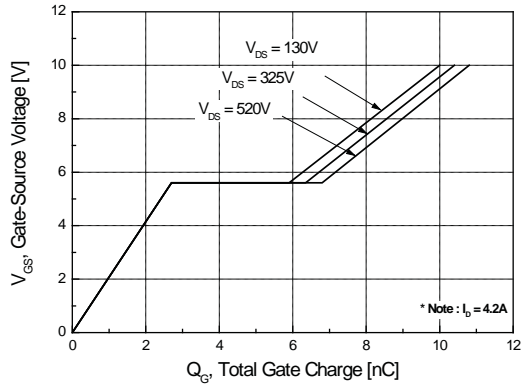


Figure 6. Gate Charge Characteristics

Typical Characteristics (continued)

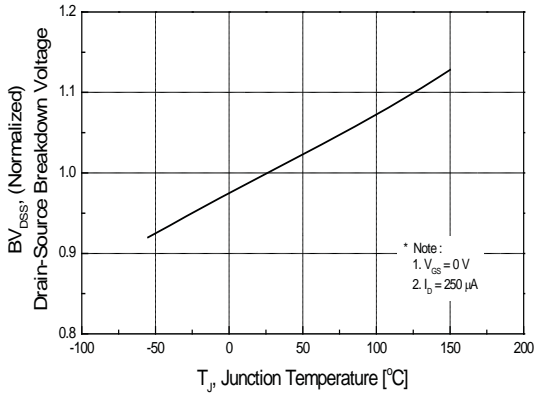


Figure 7. Breakdown Voltage Variation vs Temperature

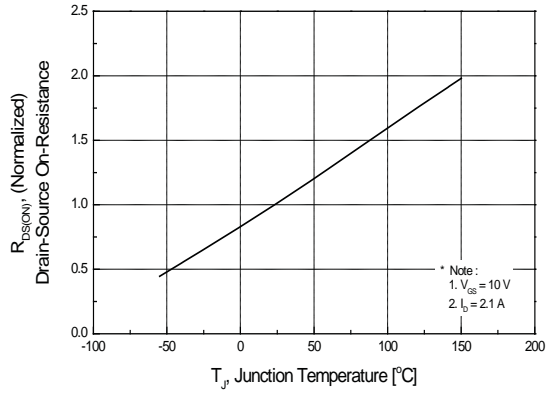


Figure 8. On-Resistance Variation vs Temperature

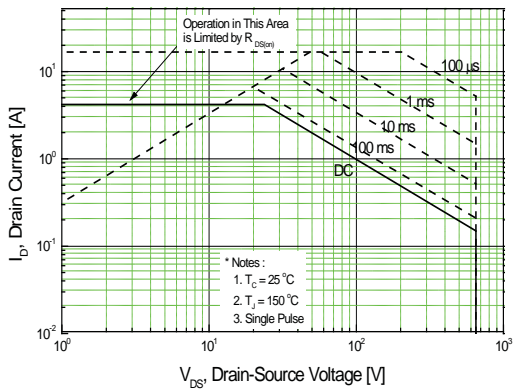


Figure 9. Maximum Safe Operating Area

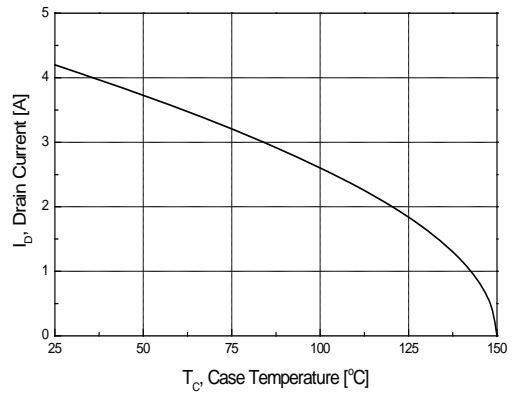


Figure 10. Maximum Drain Current vs Case Temperature

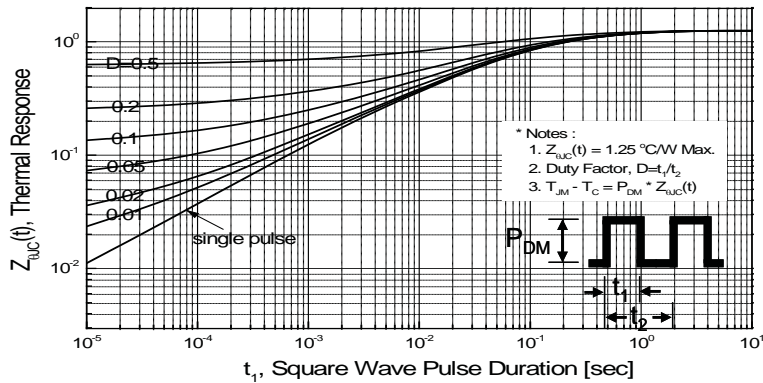


Figure 11. Transient Thermal Response Curve

**Fig 12. Gate Charge Test Circuit & Waveform**



**Fig 13. Resistive Switching Test Circuit & Waveforms**



**Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms**

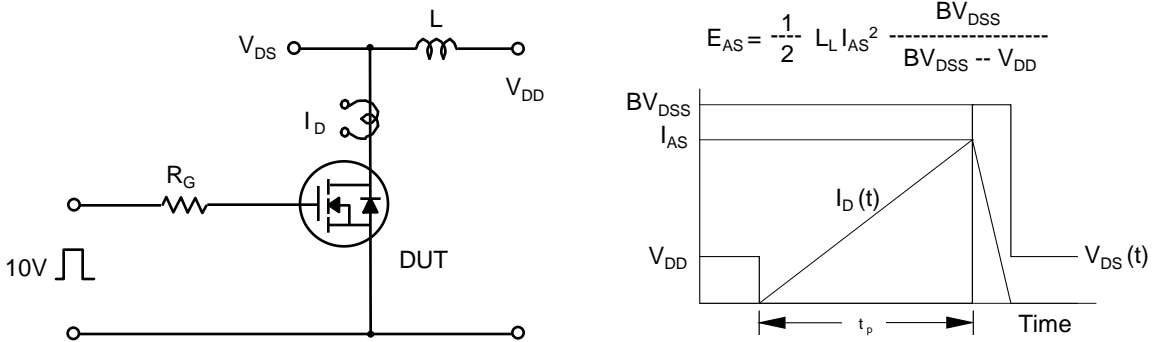
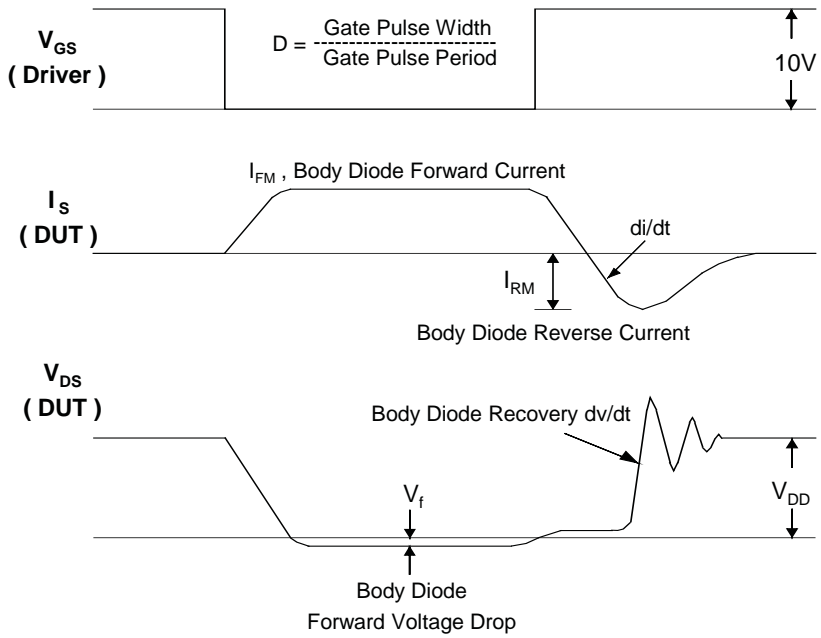
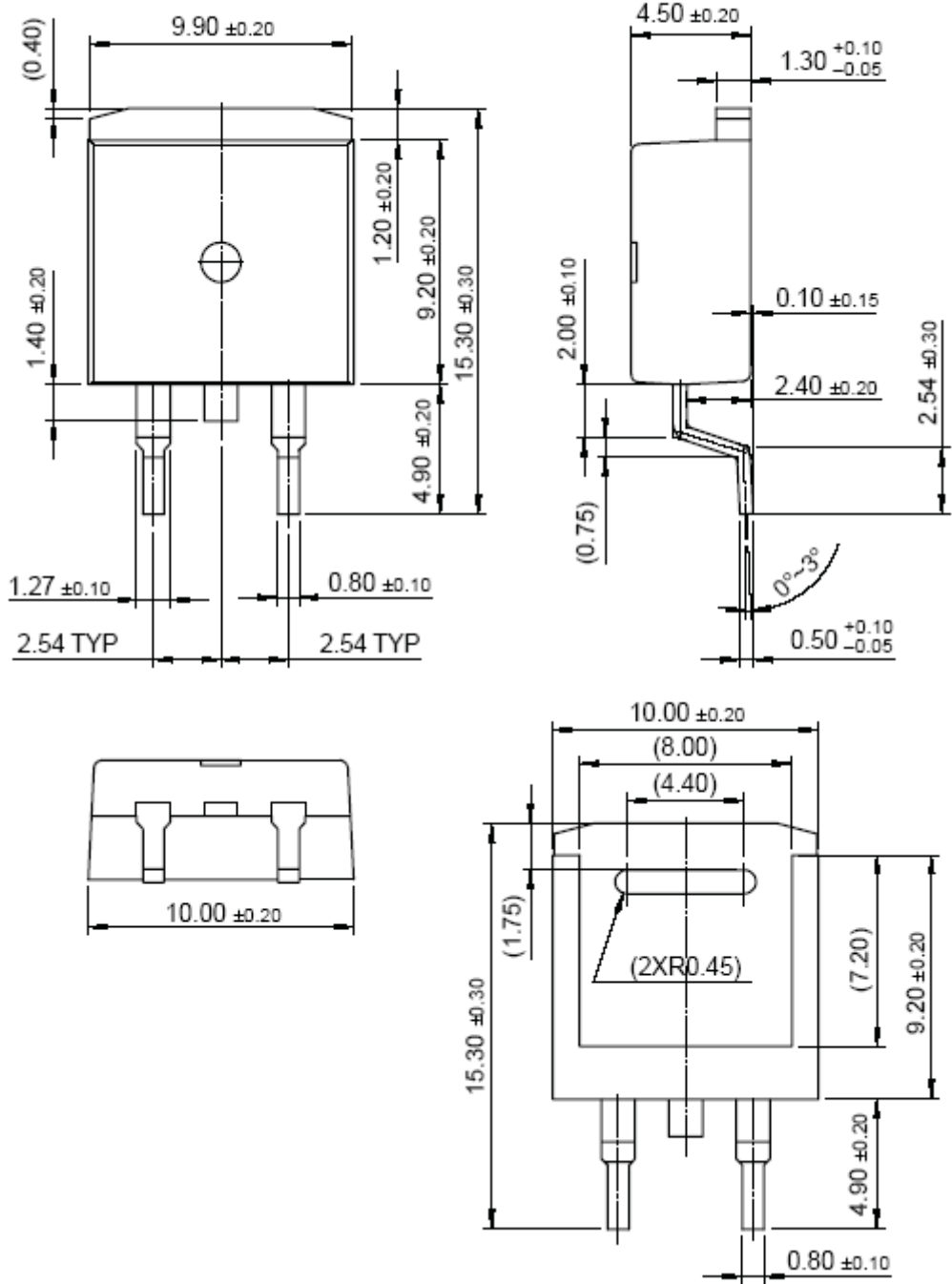


Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms



Package Dimension

D<sup>2</sup>PAK



Package Dimension

I<sup>2</sup>PAK

